

NCE N-Channel Enhancement Mode Power MOSFET

Description

The NCE0240F uses advanced trench technology and design to provide excellent RDS(ON) with low gate charge. It can be used in a wide variety of applications.

General Features

- V_{DS} =200V, I_{D} =40A $R_{DS(ON)}$ <41m Ω @ V_{GS} =10V
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

100% UIS TESTED! 100% ΔVds TESTED!



Schematic diagram



Marking and pin assignment



TO-220F top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE0240F	NCE0240F	TO-220F	-	-	-

Absolute Maximum Ratings (T_A=25 ℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	200	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I _D	40	А
Drain Current-Continuous(T _C =100℃)	I _D (100℃)	28	Α
Pulsed Drain Current	I _{DM}	160	Α
Maximum Power Dissipation	P _D	60	W
Derating factor		0.4	W /℃
Single pulse avalanche energy (Note 5)	E _{AS}	480	mJ
Operating Junction and Storage Temperature Range	T_{J} , T_{STG}	-55 To 175	$^{\circ}$ C

Thermal Characteristic

Thermal Resistance,Junction-to-Case ^(Note 2)	R _{eJC}	2.5	°C/W
Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{ heta JA}$	60	°C/W



Electrical Characteristics (T_A=25 °C unless otherwise noted)

Parameter	Symbol	Condition	Min	Тур	Max	Unit
Off Characteristics	·					
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	200	220	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =200V,V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V,V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)	·					
Gate Threshold Voltage	V _{GS(th)}	$V_{DS}=V_{GS}$, $I_{D}=250\mu A$	2	3.2	4	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =20A	-	36.4	41	mΩ
Forward Transconductance	g FS	V _{DS} =25V,I _D =25A	26	-	-	S
Dynamic Characteristics (Note4)	·					
Input Capacitance	C _{lss}		-	6500	-	PF
Output Capacitance	Coss	V_{DS} =25V, V_{GS} =0V, F=1.0MHz	-	290	-	PF
Reverse Transfer Capacitance	C _{rss}	F=1.UIVIDZ	-	220	-	PF
Switching Characteristics (Note 4)	·					
Turn-on Delay Time	t _{d(on)}		-	26	-	nS
Turn-on Rise Time	t _r	V_{DD} =30V, R_L =15 Ω	-	24	-	nS
Turn-Off Delay Time	t _{d(off)}	V_{GS} =10V, R_{G} =2.5 Ω	-	91	-	nS
Turn-Off Fall Time	t _f		-	39	-	nS
Total Gate Charge	Qg	V -20VI -20A	-	163		nC
Gate-Source Charge	Q _{gs}	V_{DS} =30V, I_{D} =30A, V_{GS} =10V	-	31		nC
Gate-Drain Charge	Q_{gd}	V _{GS} =10V	-	64		nC
Drain-Source Diode Characteristics	•					•
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V,I _S =40A	-		1.2	V
Diode Forward Current (Note 2)	Is		-	-	40	Α
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = 40A	-	42		nS
Reverse Recovery Charge	Qrr	$di/dt = 100A/\mu s^{(Note3)}$	-	66		nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

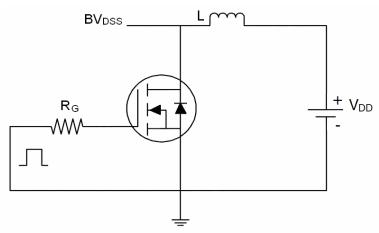
Notes:

- $\textbf{1.} \ \textbf{Repetitive Rating: Pulse width limited by maximum junction temperature.}$
- 2. Surface Mounted on FR4 Board, t ≤ 10 sec.
- 3. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2%.
- **4.** Guaranteed by design, not subject to production
- **5.** E_{AS} condition: Tj=25 $^{\circ}\text{C}$, V_{DD} =50 V, V_{G} =10 V, L=1 mH, Rg=25 Ω

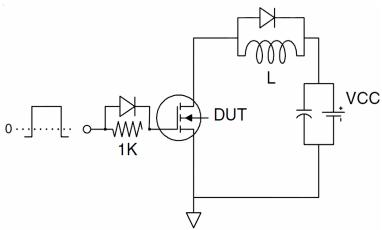


Test Circuit

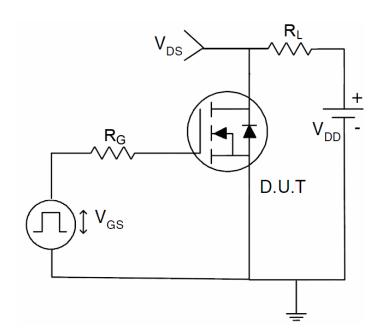
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit





Typical Electrical and Thermal Characteristics (Curves)

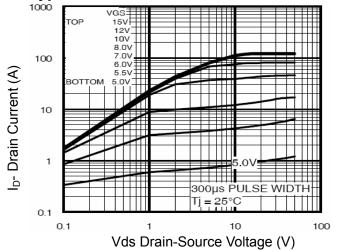


Figure 1 Output Characteristics

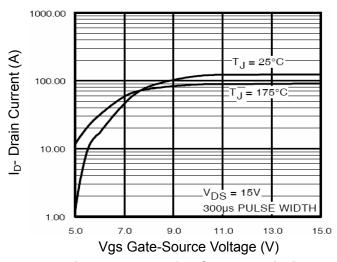


Figure 2 Transfer Characteristics

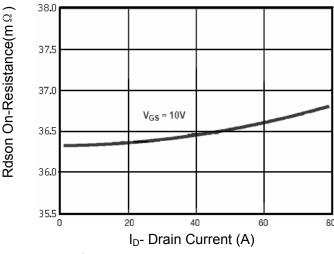


Figure 3 Rdson- Drain Current

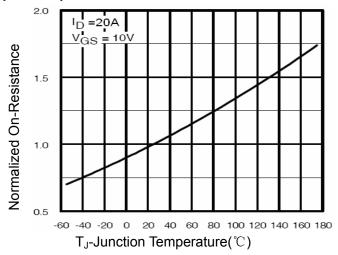


Figure 4 Rdson-JunctionTemperature

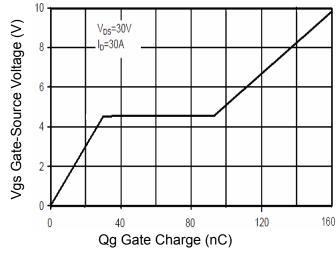


Figure 5 Gate Charge

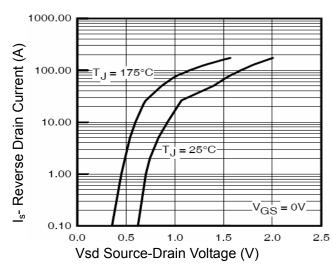


Figure 6 Source- Drain Diode Forward



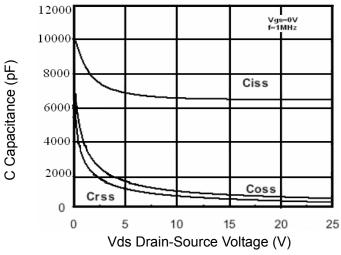


Figure 7 Capacitance vs Vds

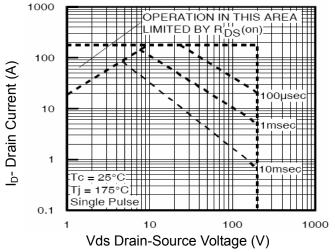


Figure 8 Safe Operation Area

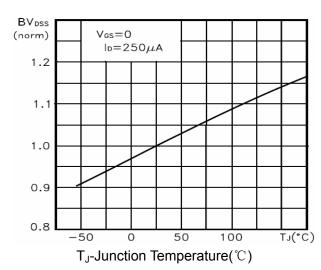


Figure 9 BV_{DSS} vs Junction Temperature

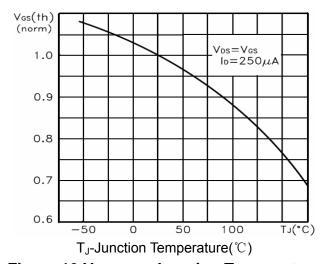


Figure 10 V_{GS(th)} vs Junction Temperature

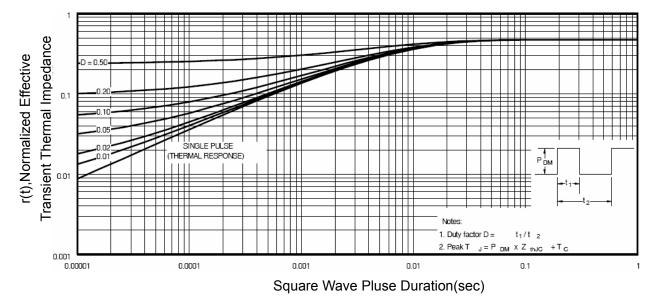
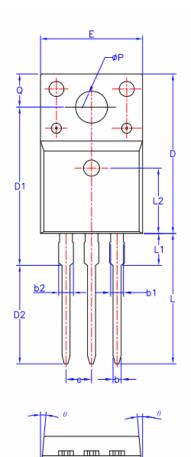
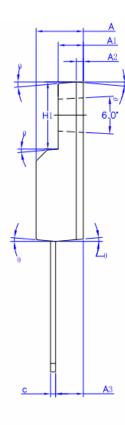


Figure 11 Normalized Maximum Transient Thermal Impedance



TO-220F Package Information





SYMBOL	MIN	NOM	MAX	
Α	4.50	4.70	4.83	
A1	2.34	2.54	2.74	
A2	0.70 REF			
A3	2.56	2.76	2.93	
b	0.70	_	0.90	
b1	1.18	_	1.38	
b2	_	_	1.47	
С	0.45	0.50	0.60	
D	15.67	15.87	16.07	
D1	15.55	15.75	15.95	
D2	9.60	9.80	10.0	
Е	9.96	10.36		
е	2.54BSC			
H1	6.48	6.68	6.88	
L	12.68	12.98	13.28	
L1	_	_	3.50	
L2	6.50REF			
ØΡ	3.08	3.18	3.28	
Q	3.20	_	3.40	
θ 1	1°	3°	5°	



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